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10/623,173	07/21/2003	Michael John Erickson	10981624-2	2724

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EXAMINER	
PHAN, RAYMOND NGAN	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 09/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

(9)

Office Action Summary	Application No.	Applicant(s)	
	10/623,173	ERICKSON ET AL.	
	Examiner	Art Unit	
	Raymond Phan	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-23 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-23 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 07212003.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Part III DETAILED ACTION

Notice to Applicant(s)

1. This application has been examined. Claims 1-23 are pending.

2. The Group and/or Art Unit location of your application in the PTO has changed. To aid in correlating any papers for this application, all further correspondence regarding this application should be directed to Group Art Unit 2111.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Double Patenting

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321© may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claim 12 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 7 respectively in Patent No. 6,625,681. Although the conflicting claims are not identical, they are not patentably distinct from each other because the omissions of,

a threshold voltage connected to a (-) input of a first comparator and to a (+) input of the second comparator, whereby said (+) input of the first comparator and said (-) input of the second comparator receive a control signal,

in claim 7 respectively are obvious expedients since elements of claim 12 the present application still includes the elements of,

a plurality of transistors connected in parallel having at least two inputs and at least one output;

at least one other transistor having at least one output and at least one input connected to said at least one output of said plurality of transistors connected in parallel;

at least one Schmitt trigger inverter having an input connected to said output of said at least one other transistor;

and a time extender circuit connected to said at least one output of said at least one other transistor,

as claim 7 of the patent. In re Karlson, 136 USPQ 189 (ccPA 1963).

6. Claim 14 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 8 respectively in Patent No. 6,625,681. Although the conflicting claims are not identical, they are not patentably distinct from each other because the omissions of,

receiving a control signal at a (+) input of a first comparator and to a (-) input of the second comparator, wherein a threshold voltage is connected to said (-) input of the first comparator and said (+) input of the second comparator,

in claim 8 respectively are obvious expedients since elements of claim 14 the present application still performs the functions of,

receiving at least one input signal indicating the insertion and removal of a circuit board;

processing said at least one input signal indicating the insertion and removal of a circuit board;

generating an output signal indicating said insertion and said removal of said circuit board;

and extending said output signal for a period of time after said circuit board is completely inserted and removed,

as claim 8 of the patent. In re Karlson, 136 USPQ 189 (ccPA 1963).

7. Claim 21 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 9 respectively in Patent No. 6,625,681. Although the conflicting claims are not identical, they are not patentably distinct from each other because the omissions of,

receiving a control signal at a (+) input of a first comparator and to a (-) input of the second comparator, wherein a threshold voltage is connected to said (-) input of the first comparator and said (+) input of the second comparator,

in claim 9 respectively are obvious expedients since elements of claim 21 the present application still performs the functions of,

outputting a plurality of complementary control signals;

performing a logic operation using one of said complementary control signals and an input signal to produce an output;

using said output from said logic operation to source current;

sinking current using said input signal.

as claim 9 of the patent. In re Karlson, 136 USPQ 189 (ccPA 1963).

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1-5, 14-15, 17-23 are rejected under 35 U.S.C. § 102(b) as being anticipated by Busby (US No. 4,245,270).

In regard to claim 1, Busby discloses an apparatus for indicating the insertion and removal of a circuit board for hot swap applications comprising: a logic circuit (G1, G2) having at least one input (21, 26, 24, 25) and at least one output (31) (see figure 1, col. 2, line 60 through col. 3, line 14); and a time extender circuit (i.e. RC circuit) (R3, C2) connected to said logic circuit, for extending an output signal of said logic circuit for a period of time after said circuit board is completely inserted and removed (see figure 1, col. 3, lines 26-65).

In regard to claim 2, Busby discloses wherein said logic circuit further comprises a NAND gate (see col. 2, lines 60-65).

In regard to claim 3, Busby discloses wherein said NAND gate further comprises: a plurality of transistors connected in parallel having a plurality of inputs and at least one output (see figure 1, col. 2, lines 60-67).

In regard to claim 4, Busby further discloses an enable logic gate (G3) connected to said at least one output of said logic circuit (see figure 1, col. 3, lines 1-7).

In regard to claim 5, Busby further discloses a transistor configured as an open collector having an input and an output whose input is connected to said at least one output of said logic circuit (see col. 2, line 60 through col. 3, line 14).
In regard to claim 6, Busby discloses wherein said time extender circuit further comprises: a resistor connected between ground and said logic circuit; and a capacitor connected between a voltage and said logic circuit (see col. 3, line 26 through col. 4, line 22).

In regard to claim 14, Busby discloses a method for indicating the insertion and removal of a circuit board, comprising: receiving at least one input signal indicating the insertion and removal of a circuit board (see col. 4, lines 22-64); processing said at least one input signal indicating the insertion and removal of a circuit board (see col. 4, lines 22-64); generating an output signal indicating said insertion and said removal of said circuit board (see col. 4, lines 22-64); and extending said output signal for a period of time after said circuit board is completely inserted and removed (see col. 4, line 29 through col. 5, line 41).

In regard to claim 15, Busby further discloses the step of enabling said output signal (i.e. output signal from G3) (see figure 1, col. 4, lines 3-64).

In regard to claim 17, Busby discloses wherein said step of extending said output signal for a period of time after said circuit board is completely inserted or

extracted further comprises the step of discharging a capacitor (see col. 5, lines 31-41).

In regard to claims 18, 21, Busby further comprising the steps of: outputting a plurality of complementary control signals (see col. 4, lines 3-64); performing a logic operation using one of said complementary control signals and said output signal to produce a logic output (see col. 4, lines 3-64); using said logic output from said logic operation to source current (see col. 4, lines 3-64); and sinking current using said output signal (see col. 4, lines 3-64).

In regard to claim 19, Busby discloses wherein said step of processing further comprises the step of performing a logic function on said at least one input signal (see col. 4, lines 3-64).

In regard to claim 20, Busby discloses wherein said logic function further comprises the step of performing a NAND logic function on said at least one input signal (see col. 4, lines 3-64).

In regard to claim 22, Busby discloses wherein said step of sinking current further comprises using another of said plurality of complementary control signals to sink said current to ground or through a resistor to ground (see col. 5, lines 42-59).

In regard to claim 23, Busby discloses wherein said step of outputting a plurality of complementary control signals further comprises applying a threshold voltage (see col. 3, lines 9-40).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 7-13, 16 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Busby in view of Nakaoka (US No. 4,886,984).

In regard to claim 7, Busby discloses the claimed subject matter as discussed above rejection except the teaching of at least one inverter having an input and an output, wherein said input of said at least one inverter is connected to an output of said NAND gate. However Nakaoka discloses at least one inverter 48 having an input and an output, wherein said input of said at least one inverter is connected to an output of said NAND gate 47 (see figure 3, col. 6, lines 43-64). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Nakaoka within the system of Busby because it would provide a prohibition circuit upon power on event which prohibits power consuming circuits from undesirable operation after the power switch on event.

In regard to claim 8, Nakaoka further discloses at least one inverter having an input and an output, wherein said input of said at least one inverter is connected to said at least one output of said plurality of transistors (see figure 3, col. 6, lines 43-64). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Nakaoka within the system of Busby because it would provide a prohibition circuit upon power on event which prohibits power consuming circuits from undesirable operation after the power switch on event.

In regard to claims 9-10, even though the teachings of Nakaoka does not disclose the inverter is a Schmitt trigger inverter, however one skilled in the art

would have understood that they can choose to have different type of inverter to fulfill their need.

In regard to claim 11, Nakaoka further discloses an enable logic gate connected to at least one of said outputs of said at least one inverter; and a transistor configured as an open collector having an input and an output whose input is connected to at least one of said outputs of said at least one inverter (see figure 3, col. 6, lines 43-64). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Nakaoka within the system of Busby because it would provide a prohibition circuit upon power on event which prohibits power consuming circuits from undesirable operation after the power switch on event.

In regard to claim 12, Busby discloses an apparatus for indicating the insertion and removal of a circuit board, comprising: a plurality of transistors (G1, G2) connected in parallel having at least two inputs (21, 26, 24, 25) and at least one output (31) (see figure 1, col. 2, line 60 through col. 3, line 24); at least one other transistor (G3) having at least one output and at least one input connected to said at least one output of said plurality of transistors connected in parallel (see figure 1, col. 2, line 60 through col. 3, line 24); a time extender circuit (i.e. RC circuit (R3, C2) connected to said at least one output of said at least one other transistor (see figure 1, col. 3, lines 26-65). But Busby does not specifically disclose at least one inverter having an input connected to said output of said at least one other transistor. However Nakaoka discloses at least one inverter 48 having an input and an output, wherein said input of said at least one inverter is connected to an output of said NAND gate 47 (see figure 3, col. 6, lines 43-64). Therefore, it would have been obvious to a person of an ordinary skill in the art at

the time the invention was made to have combined the teachings of Nakaoka within the system of Busby because it would provide a prohibition circuit upon power on event which prohibits power consuming circuits from undesirable operation after the power switch on event.

In regard to claim 13, Nakaoka further discloses a transistor configured as an open collector having an input and an output whose input is connected to said output of said at least one inverter (see figure 3, col. 6, lines 43-64). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Nakaoka within the system of Busby because it would provide a prohibition circuit upon power on event which prohibits power consuming circuits from undesirable operation after the power switch on event.

In regard to claim 16, Nakaoka further discloses the step of inverting said output signal (see figure 3, col. 6, lines 43-64). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Nakaoka within the system of Busby because it would provide a prohibition circuit upon power on event which prohibits power consuming circuits from undesirable operation after the power switch on event.

Conclusion

12. All claims are rejected.

13. The prior arts made of record and not relied upon are considered pertinent to applicant's disclosure.

Erickson et al. (US No. 6,487,624) disclose a method and apparatus for hot swapping and bus extension without data corruption.

Parrett (US No. 5,586,271) discloses an in-line SCSI bus circuit for providing isolation and bi-directional communication between two portions of a SCSI bus.

Ahn et al. (US No. 5,202,965) disclose an electronic system with a plurality of removable units.

Carey et al. (US No. 5,758,102) disclose a soft switching circuit fo ruse on backplane.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Raymond Phan, whose telephone number is (703) 306-2756. The examiner can normally be reached on Monday-Friday from 6:30AM- 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's Primary, Paul Myers can be reached on (703) 305-9656 or via e-mail addressed to paul.myers@uspto.gov. The fax phone number for this Group is (703) 872-9306.

Communications via Internet e-mail regarding this application, other than those under 35 U.S.C. 132 or which otherwise require a signature, may be used by the applicant and should be addressed to [**raymond.phan@uspto.gov**].

All Internet e-mail communications will be made of record in the application file. PTO employees do not engage in Internet communications where there exists a possibility that sensitive information could be identified or exchanged unless the record includes a properly signed express waiver of the confidentiality requirements of 35 U.S.C. 122. This is more clearly set forth in the Interim Internet Usage Policy published in the Official Gazette of the Patent and Trademark on February 25, 1997 at 1195 OG 89.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Paul R. Myers

PAUL R. MYERS
PRIMARY EXAMINER

Raymond Phan
9/10/04